UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/883,373	06/19/2001	Eiji Hasegawa	NEC01P075-AMb	1068

466 7590 05/08/2003

YOUNG & THOMPSON
745 SOUTH 23RD STREET 2ND FLOOR
ARLINGTON, VA 22202

EXAMINER
BEREZNY, NEAL

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 05/08/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/883,373	Applicant(s) HASEGAWA, EIJI	
	Examiner Neal Berezny	Art Unit 2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 February 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *04 February 2003* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

2. The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims 1 and 2 rejected under 35 U.S.C. 102(e) as being anticipated by Houlihan et al. (6,258,673). Houlihan teaches a method of manufacturing a semiconductor device having a plurality of gate insulating films of different thicknesses on a semiconductor substrate, Fig.4, el.22, 24, 26, and 28, comprising the steps of: injecting fluorine into a region of a semiconductor substrate other than a region of the semiconductor substrate where a thinnest gate insulting film is to be formed, among a plurality of regions where gate insulating films are to be formed; fig.2, col.2, ln.37-42, oxidizing the semiconductor substrate with fluorine injected therein to form an oxide film in said plurality of regions; col.3, ln.9-21, nitriding an exposed surface of said oxide film to turn an exposed surface layer thereof into an oxynitride film or to form a nitride film on

the exposed surface of said oxide film; col.3, ln.18-21, wherein said step of injecting fluorine comprises the step of setting conditions for injecting fluorine such that the gate insulating films formed on said semiconductor substrate have a thickness difference of at least 0.2 nm; col.4, ln.47-53.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Houlihan as applied to claims 1 and 2 above, and further in view of Applicant's Admitted Prior Art (AAPA). Houlihan also teaches forming a first oxide film on a surface of a semiconductor substrate; fig.1, el.20. Houlihan appears not to specifically recite the step of removing said first oxide film from regions of the semiconductor substrate other than a region of the semiconductor substrate where a thickest gate insulating film is to be formed, among a plurality of regions where gate-insulating films are to be formed. AAPA teaches implanting fluorine directly into the silicon substrate, wherein any previously grown oxide had been removed, fig.1b. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine AAPA with Houlihan to modify the Houlihan process to implant the fluorine directly into the substrate rather than through an oxide layer. It is well known in the art to implant directly into the substrate,

but this can cause ion channeling, thus implants are often done through an oxide to prevent channeling, which in some cases damages the oxide, thus the oxide is often removed and then regrown. Note that Houlihan grows an oxide, which is then masked and protected from implants, fig.3, el.300. It would be obvious to implant without a sacrificial oxide so as to obtain a deeper implant and cause greater crystal damage to further enhance the oxidation growth rate of the region.

6. Claims 3 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Houlihan and AAPA as applied to claims 1-2, 4-5 above, and further in view of Rodder et al.(6,251,761). Houlihan and AAPA do not teach the use of a remote nitrogen plasma for nitriding the gate oxide. Rodder teaches using remote plasma nitrogen for nitriding a gate oxide, col.3, ln.25-34. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Rodder with Houlihan and AAPA to use a nitrogen plasma on the oxide to form a barrier layer from Boron contaminants and to prevent oxidation of the subsequent formation of the gate electrode, which would degrade the capacitance of the gate, col.3, ln.3-6.

7. Claims 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Houlihan, AAPA, and Rodder as applied to claims 1-6 above, and further in view of DeBusk et al.(6,140,187). Although Houlihan and Rodder do teach the formation of a gate stack, fig.4, el.105, 205, 305, and 405, and fig.2d and fig.1, el.104, respectively, the combination of Houlihan, AAPA, and Rodder do not specifically state the specific well known steps involved in building a gate stack containing a gate insulator and a polysilicon gate electrode, nor the well known method of forming different gate

thicknesses by forming gate stacks and then removing them from all but the desired regions, and then forming a new gate stack in the removed region with the second desired gate thickness. DeBusk teaches the steps for forming a gate stack, and the strategy of forming the well known method of forming different gate thicknesses by forming gate stacks and then removing them from all but the desired regions, and then forming a new gate stack in the removed region with the second desired gate thickness, fig.1, el.160 and 140, fig.2, el.260 and 270, col.4, ln.27-41. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Debusk with AAPA and Rodder to employ these well known methods of forming a gate stack to obtain gate insulators with different thicknesses, so that devices of different types could be manufactured on the same substrate with the same process, thereby reducing costs.

Response to Arguments

8. Applicant's arguments with respect to claims 1-9 have been considered but are moot in view of the new ground(s) of rejection.

CONCLUSION

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Neal Berezny whose telephone number is (703) 305-1481. The examiner can normally be reached on M-F 9:00 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (703) 306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7724 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Olik Chaudhuri
Supervisory Patent Examiner
Technology Center 2800

NB
April 25, 2003